



**THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Cheng-Lien Chiang  
Assignee: Bridge Semiconductor Corporation  
Title: OPTOELECTRONIC SEMICONDUCTOR PACKAGE DEVICE  
Serial No.: 10/082,500 Filed: February 25, 2002  
Examiner: Chu, C. Group Art Unit: 2815  
Atty. Docket No.: BDG005-3

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COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PETITION FOR WITHDRAWAL OF SPECIFICATION OBJECTION  
FOR LACK OF BRIEF DESCRIPTION OF FIGS. 1A-14B**

Dear Sir:

This Petition is filed under 37 C.F.R. § 1.181 to request that the outstanding requirement to provide a brief description of Figs. 1A-14B be withdrawn.

**I. FACTS**

Figs. 1A-14A and 1B-14B are bottom and top perspective views, respectively, of a method of making an optoelectronic semiconductor package device.

The Specification provides a brief description of Figs. 1A to 14B in the Brief Description of the Drawings as follows:

FIGS. 1A-14A are bottom perspective views that show a method of making an optoelectronic semiconductor package device in accordance with an embodiment of the present invention;

FIGS. 1B-14B are top perspective views corresponding to FIGS. 1A-14A, respectively; (Page 6, lines 4-7.)

The Office Action dated April 10, 2003 objects to the Specification as follows:

On page 7, the specification needs a brief description of the drawings for Figs. 13A ~ 14B.

Appropriate correction is required.

The Response dated April 24, 2003 requested that the objection be withdrawn.

The Office Action dated July 31, 2003 maintained the objection as follows:

On page 7, the specification needs a brief description of the drawings for Figs. 1A ~ 14B.

Appropriate correction is required.

However, the sentence "FIGS. 1A-14A are bottom perspective views that show a method of making an optoelectronic semiconductor package device in accordance with an embodiment of the present invention" is not clear or accurate description for the brief description of the drawings.

## II. ARGUMENT

The Brief Description of the Drawings need not describe each figure individually. For instance, no such requirement exists in the Rules or the Manual of Patent Examining Procedure. See 37 C.F.R. § 1.74 and M.P.E.P. § 608.01(f).

Furthermore, it is common for the brief description of the drawings to summarize multiple figures without describing each figure individually. See, for instance, *Maekawa* (U.S. Patent No. 5,834,835), *Mori et al.* (U.S. Patent No. 5,834,843), *Kuraishi et al.* (U.S. Patent No. 5,859,471), *Fjelstad* (U.S. Patent No. 6,001,671) and *Tsuji et al.* (U.S. Patent No. 6,025,650), all cited by the Examiner.

*Maekawa* provides a brief description of the drawings as follows:

FIG. 3A to FIG. 3F are cross sectional views each showing the steps of a method of manufacturing a semiconductor device including a conventional enclosure; (Col. 4, lines 28-30.)

FIG. 6A to FIG. 6F are cross sectional views each showing the steps of a method of manufacturing a semiconductor device including an enclosure of the present invention; (Col. 4, lines 36-39.)

*Mori et al.* provides a brief description of the drawings as follows:

FIGS. 2A-2D are diagrams showing the structure of various multi-chip modules; (Col. 3, lines 35-36.)

FIGS. 10A-10D are diagrams showing various cooling schemes of the multi-chip module of the first embodiment; (Col. 3, lines 58-59.)

FIGS. 13A-13D are diagrams showing the fabrication process of the multi-chip module of the first embodiment; (Col. 3, lines 66-67.)

*Kuraishi et al.* provides a brief description of the drawings as follows:

FIGS. 1A-1D are plan views of some embodiments of a lead frame according to the present invention; (Col. 3, lines 47-48.)

FIGS. 2A-2D are plan views of embodiments of a semiconductor device, using a lead frame shown in FIGS. 1A-1D, respectively, according to the present invention; (Col. 3, lines 49-51.)

FIGS. 6A-6D are cross-sectional views of some variations of an inner lead-bonding type semiconductor device according to the present invention; (Col. 3, lines 59-61.)

FIGS. 9A-9D are cross-sectional views of some variations of a potted type semiconductor device; (Col. 4, lines 1-2.)

*Fjelstad* provides a brief description of the drawings as follows:

FIGS. 1A through 1G-1 show a side view of a method of manufacturing a semiconductor chip package, according to the present invention. (Col. 2, lines 63-65.)

FIGS. 2A through 2E show a side view of an alternate method of manufacturing a semiconductor chip package, according to the present invention. (Col. 3, lines 7-9.)

FIGS. 5A through 5H show a side view of an alternate method of manufacturing a semiconductor chip package, according to the present invention. (Col. 3, lines 24-26.)

FIGS. 7A through 7E show a side view of an alternate method of manufacturing a semiconductor chip up to the encapsulation step, according to the present invention. (Col. 3, lines 41-43.)

*Tsuji et al.* provides a brief description of the drawings as follows:

FIGS. 16A, 16B, 16C and 16D are schematic illustrations showing a method for producing a pattern portion of the second embodiment; (Col. 8, lines 42-44.)

FIGS. 19A, 19B and 19C are schematic illustrations showing a method for producing the semiconductor device of the third embodiment of the present invention; (Col. 8, lines 52-54.)

FIGS. 20A, 20B and 20C are schematic illustrations showing a continuation of the method for producing the semiconductor device of the third embodiment of the present invention; (Col. 8, lines 56-59.)

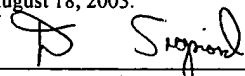
FIGS. 24A, 24B and 24C are schematic illustrations showing a continuation of the method for producing the semiconductor device of the fourth embodiment; (Col. 9, lines 1-3.)

FIGS. 28A, 28B, 28C and 28D are schematic illustrations showing a method for producing the semiconductor device of the fifth embodiment; (Col. 9, lines 1-3.)

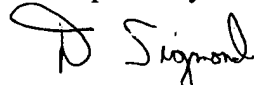
Therefore, the Brief Description of the Drawings accurately and concisely describes Figs. 1A to 14B. The Examiner's assertion that the Brief Description of the Drawings is not clear or accurate is unsupported and inconsistent with numerous patents the Examiner has cited that summarize multiple figures without describing each figure individually.

Therefore, Applicant requests that this objection be withdrawn.

Please charge any fee due under this Petition to Deposit Account No. 502178/BDG005-3.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 18, 2003.	
	<u>8, 18, 03</u>
David M. Sigmond Attorney for Applicant	Date of Signature

Respectfully submitted,



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